R E M A R K S

Reconsideration of this application, as amended, is respectfully requested.

RE: INFORMATION DISCLOSURE STATEMENT (IDS)

It is respectfully requested that the Examiner return signed and initialed copies of the IDS forms dated April 27, 2005 (2 pages), January 7, 2008 (1 page), September 23, 2008 (3 pages) and September 24, 2008 (1 page), in order to confirm that the documents cited therein have all been considered and made of record.

THE CLAIMS

Independent claim 1 has been amended to incorporate subject matter formerly recited in claim 27 and (now canceled) claim 26. See, for example, the disclosure in Fig. 25 (Fig. 6) and the corresponding disclosure in the specification. Similarly, independent method claim 64 has been amended to incorporate subject matter formerly recited in claim 73 and (now canceled) claim 72.

In addition, claims 27 and 28 have been amended to directly depend from claim 1, and claim 73 has been amended to depend directly from method claim 64. The claims have also been amended throughout to remove the reference numerals cited therein, and

claims 12, 15 and 65 have been amended to recite "2^n" (2 raised to the power n) instead of reciting "2n" (2 × n) so as to accord with the disclosure in the specification.

Still further, the claims have been amended to make some minor grammatical improvements and to correct some minor antecedent basis problems so as to put them in better form for issuance in a U.S. patent.

Withdrawn claims 40-63, moreover, have been canceled, without prejudice.

No new matter has been added, and it is respectfully requested that the amendments to the claims be approved and entered.

THE PRIOR ART REJECTION

Claims 1-5, 9, 12, 13, 16-18, 20-23, 26, 27, 35 and 36 were rejected under 35 USC 102 as being anticipated by US 2003/0040149 ("Kasai"); and claims 6, 7, 10, 11, 24, 25, 28, 29, 37 and 64-73[1] were rejected under 35 USC 103 as being obvious in view of the combination of Kasai and USP 6,528,951 ("Yamazaki et al"). These rejections, however, are respectfully traversed with respect to the claims as amended hereinabove.

[1] It is noted that the Examiner incorrectly indicated on the Office Action Summary sheet that claim 73 has been withdrawn from consideration. However, claim 73 has been elected and the Examiner correctly acted on claim 73 in the body of the Office Action.

According to the present invention as recited in amended independent claim 1, a display device is provided for displaying image information corresponding to display signals derived from digital signals. As recited in amended independent claim 1, the display device comprises a display panel comprising a plurality of signal lines and a plurality of scanning lines which intersect perpendicularly with each other and a plurality of display pixels with optical elements arranged near intersecting points of the plurality of signal lines and the plurality of scanning lines, a scanning driver circuit for sequentially applying a scanning signal to each of plurality of the scanning lines for setting the plurality of display pixels in a selective state a line at a time, and a signal driver circuit comprising a plurality of current generation circuits.

Significantly, as recited in amended independent claim 1, each of the current generation circuits comprises: (i) a gradation current generation circuit which generates a plurality of gradation currents corresponding to each bit of the display signals based on a predetermined constant reference current, (ii) a drive current generation circuit which generates a drive current that is selected based on the plurality of gradation currents corresponding to each bit of the display signals, and that is supplied to a corresponding signal line, and (iii) a specified state setting circuit which supplies a specified

voltage to the corresponding signal line to drive the corresponding optical element in a specified operating state instead of supplying the generated drive current, when the display signals have a specified value that sets all of the plurality of gradation currents in a non-selection state.

Independent claim 64, moreover, recites a method for driving a display device corresponding to the above described structure recited in amended independent claim 1.

With the structure and method of the present invention as recited in amended independent claims 1 and 64, since instead of supplying the generated drive current, a (specified) voltage is supplied to the signal line at a time of minimum gradation (at a time when the display signals have a specified value that sets all of the plurality of gradation currents in a non-selection state), current flowing to the signal line is not limited and writing is carried out in a relatively rapid manner. As a result, with the structure and method of the claimed present invention, writing of the minimum gradation current is surely completed during a selection period, and an advantageous effect is produced whereby the panel is controlled by the appropriate luminosity gradations corresponding to the display signals and a markedly better display quality is achieved.

It is respectfully submitted that Kasai and Yamazaki et al, even if considered in combination, do not achieve or render

obvious the above described claimed structural features and advantageous effects of the present invention as recited in amended independent claims 1 and 64.

In particular, Kasai discloses a display device comprising a display panel, a scan line drive circuit and a data line drive circuit. In Kasai, the data line drive circuit has a plurality of single line drivers 300 for drive each data line Xm. The single line driver 300 is provided with a D/A converter section 310 and an offset current generation circuit 320. See Fig. 5 of Kasai.

In Kasai, when 8-bit gradation data is applied to the D/A converter section 310 from the control circuit 105, the ON/OFF switching of the switching transistors 81-88 connected to each of the eight current lines IU1-IU8 is controlled in response to the value of each bit of this gradation data. A current line I_{offset} of the offset current generation circuit 320 is connected in parallel to the eight current lines IU1-IU8. And the total current flowing in the nine current lines (I_{offset} and IU1-IU8) is output to the data line 302 as a programming current.

According to Kasai, however, when the gradation data of the single line driver 300 is a value where all of the switching transistors 81-88 are turned OFF (i.e., plurality of gradation currents in non-selection state), the current I_{offset} generated by

the offset current generation circuit 320 is output on the data line 302.

By contrast, according to the present invention as recited in each of amended independent claims 1 and 64, instead of supplying the generated drive current, a specified voltage is supplied (by the specified state setting circuit) to the signal line to drive the optical element in a specified operating state, when the display signals have a specified value that sets all of the gradation currents in a non-selection state. Therefore, it is respectfully submitted that Kasai merely discloses a conventional structure and does not at all disclose or suggest the feature of the claimed present invention whereby each current generation circuit comprises a specified state setting circuit.

According to the claimed present invention, when the display signals are the specified value that sets all the gradation currents to the non-selection state, the specified voltage is supplied to the signal line (by the specific state setting circuit.) This is in contrast to Kasai where the current I_{offset} generated by the offset current generation circuit 320 is supplied (that is, the drive current is supplied) to the signal line. It is therefore respectfully submitted that Kasai cannot produce the advantageous effect of a markedly better display quality as is produced by the display panel and driving method of the claimed present invention.

More specifically, the specified value of the display signals that sets all the gradation currents in the non-selection state is when the value of all bits of the display signals is zero where the optical elements are in a minimum (lowest) gradation state representing a non-luminescent state.

As is evident from Figs. 6(a) and 6(b) of Kasai, when the single line driver 300 outputs the current I_{offset} to the data line 302, this current I_{offset} is a minute electric current having a current value less than the current value for each gradation of the gradation data.

With this method, however, when drive currents corresponding to the display signals are applied to the signal lines and a voltage corresponding to the display signals is written in the display pixels, application of the drive currents to the signal lines is accompanied by an operation which charges and discharges parasitic capacitance that is parasitic on the signal lines to the potential corresponding to the drive currents. A period of time that this charge or discharge requires is long when the current value of the drive current is small. As a result, according to Kasai which applies the current I_{offset} to the signal line at a time of minimum (lowest) gradation, a situation can occur where writing corresponding to the current I_{offset} is not completed within a predetermined selection period. In that case, the display panel of Kasai cannot be controlled by the

appropriate luminosity gradations corresponding to the display signals and causes deterioration of the display quality.

By contrast, with the structure and method of the claimed present invention, voltage is supplied (instead of supplying the drive current) to the signal line (by the specified state setting circuit) at a time of minimum gradation. And because the current which flows to the signal line is not limited when applying and writing the supplied voltage, writing of the voltage is carried out in a relatively rapid manner. For this reason, writing of the voltage is surely completed within the predetermined selection period, and the advantageous effect of the display panel being controlled by the appropriate luminosity gradations corresponding to the display signals and a markedly better display quality being achieved is produced.

It is respectfully submitted, moreover, that Yamazaki et al also does not disclose or suggest the structure of the gradation current generation circuit, drive current generation circuit, specified state setting circuit and corresponding functional limitations and advantageous effects of the present invention as recited in amended independent claims 1 and 64.

Accordingly, it is respectfully submitted that even if Kasai and Yamazaki et al were combinable in the manner suggested by the Examiner, such combination still would not achieve or render obvious the features, functional limitations and advantageous

effects of the current generation circuit of the present invention as recited in amended independent claims 1 and 64.

In view of the foregoing, it is respectfully submitted that the present invention as recited in amended independent claims 1 and 64, and all the claims respectively depending therefrom (including the withdrawn dependent claims), clearly patentably distinguishes over Kasai and Yamazaki et al, taken singly or in combination, under 35 USC 102 as well as under 35 USC 103.

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Entry of this Amendment, allowance of the claims and the passing of this application to issue are respectfully solicited.

If the Examiner has any comments, questions, objections or recommendations, the Examiner is invited to telephone the undersigned for prompt action.

Respectfully submitted,

/Douglas Holtz/

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